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09/697,419	10/26/2000	Alan McNutt	99 P 7938 US 01	5374

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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/697,419	MCNUTT, ALAN	
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 5/2/2005.

As indicated in Applicant's response, claim 7 has been amended. Claims 4-11 are pending in the office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moran et al., USPN: 5, 519,843 (hereinafter Moran) in view of Stripf et al., USPN: 6,263,487 (hereinafter Stripf).

As per claim 4, Moran discloses a programmable controller (Fig. 9) lacking instructions to convert a user program from a symbolic form to a binary form, said controller comprising:

a program execution device (Fig. 3) comprising

a micro controller operable to implement the programmable controller operating system upon executing a compilation comprising the user program and a system BIOS support functions (e.g. Fig. 2, 3, 9; *user storage* ... *emulation* - col. 5, lines 36-44; col. 5, line 46 to col. 6, line 48), said system support adapted to provide said programmable controller with operating system functions comprising sequencing the user program (e.g. col. 4, lines 6-11 – Note: executing user program for implementing OS of device implicitly disclose a sequencing of steps);

said program execution device separable from a communication/programming device adapted to convert the user program to a binary code module and combine the binary module with the system support kernel into a single executable module (e.g. Fig. 2 – Note: the user program being flashed into the controller 20 and fetched by controller OS reads on separate communication/programming device adapted to translate user program into application code, or executable form, externally provided and stored into controller programmable memory – see col. 6, line 59 to col. 7, line 3);

said programmable controller lacking a memory device external to said program execution device (e.g. Fig. 5 – controller with system memory 12 comprising flashed BIOS and separated and executing independent from any external memory reads on lacking a memory device external to said execution device)

a re-programmable read-only memory within which compiled is stored (e.g. Fig. 3).

But Moran does not explicitly disclose that said programmable controller is a programmable logic controller (PLC); but an integrated controller (see Fig. 9) and the use of code to emulate more than one type of devices (see col. 7, lines 14-23) wherein a programmable memory stores user programs for effecting logic to implement the control over an OS and related functionalities as taught by Moran (see SUMMARY) suggests a form of programmable logic controller; and the concept of emulation/simulation of multiple devices requiring control is suggested. The specializing from Moran's ASIC single chip programmable controller-- into a PLC would have been obvious by virtue of the rationale using Stripf as follows.

Nor does Moran explicitly teach that the programmable controller is being implemented for executing a compilation is to implement PLC I/O functions and that the compilation

comprises system support kernel. But in view of Moran 's teachings as to be able to initialize the power settings or memory input/output resetting of the controller (e.g. col. 4, lines 16 to col. 5, line 35; Fig. 7), such kernel related support functions being inside the loaded operating system as a result of power-up input/output routines or I/O functions are strongly implied if not disclosed (see Moran: *flash memory* ... *provides* ... *operating system* - col. 2, lines 14-18; Fig. 4; *load* ... *operating system* - col. 6, lines 63-65 – Note: loaded operating system upon boot up necessarily include the core operating code for the OS loaded, and this core is commonly referred to as kernel). In case such kernel limitation is not evident from Moran's above teaching, it would have been obvious. In a system using external sources to provide compiled programs or modules to implement programmable controller operating system analogous to Moran's micro controller being flashed with user program and BIOS code, Stripf discloses a programmable logic controller (PLC) being provided with externally compiled user programs and kernel support code (e.g. watchdog Wd) as well as input/output functionalities object modules and simulation control (e.g. Fig. 2; col. 4, line 6 to col. 5, line 26; col. 3, lines 17-21). Based on the teachings by Moran for logic control of an OS and/or emulation of interconnected devices, it would have been obvious for one of ordinary skill in the art at the time the invention was made to make the controller or ASIC by Moran a form of PLC and implementing this PLC I/O functions with Stripf's object-oriented program for implementing kernel support and I/O functionality because as shown by Moran, basic I/O functions control is a fundamental part of a system power-up with a plurality of interconnected devices including error detecting routines with respect to devices connected to such controller as intended by Moran, and that according to Stripf, a PLC with such I/O functionality can provide access management to a wide interconnected bus system under

control of such micro controller (see Stripf 's BACKGROUND) and that kernel support like Stripf's watchdog can enhance the detection error during boot up as suggested in Moran's BIOS routines execution mentioned above.

Nor does Moran explicitly specify a single chip program execution device separable for a communication/programming device; but in view the teachings of user code being flashed into a single device for starting an operating system of the device (see Fig. 9; col. 6, line 59 to col. 7, line 3 – Note: Flash memory for storing ready made code reads on code being compiled outside the target code having the flash storage capability, hence reads on external communication device to burn into the flash), this limitation is disclosed.

As per claim 5, Moran discloses a method for

receiving a symbolic user program at a communication/programming device separable from a single-chip program execution device (Fig. 2 – Note: the user program being flashed into the controller 20 and fetched by controller OS reads on separate communication/programming device adapted to translate user program into application code, or executable form, externally provided and stored into controller programmable memory – see col. 6, line 59 to col. 7, line 3) having a re-programmable read only memory (Fig. 3),

said single chip device adapted to execute binary programmable logic control program program (e.g. col. 1, lines 20-24; Fig. 1; Fig. 2; col. 3, lines 9-63); such program stored in re-programmable memory (Fig. 3), and adapted to operate such programmable controller (see SUMMARY; col. 5, line 46 to col. 6, line 48),

said controller lacking a memory device separate from the single-chip execution device (e.g. Fig. 5 – controller with system memory 12 comprising flashed BIOS and separated and

executing independent from any external memory reads on lacking a memory device external to said execution device);

said symbolic user program being in a executable, i.e. binary, format loaded for execution (e.g. col. 6, line 59 to col. 7, line 3);

combining the binary code module with a system BIOS support to form said binary programmable logic control program, said system BIOS support adapted to provide said programmable controller with the operating system functions (see SUMMARY) comprising sequencing the user program (e.g. col. 6, line 59 to col. 7, line 3 - Note: executing user program for implementing OS of device implicitly disclose a sequencing of steps).

But Moran does not explicitly teach that the BIOS support functions are kernel support functions or that that the controller/ASIC single chip is PLC. However, as already been addressed in claim 4, these limitations are rejected herein using the corresponding rationale set forth therein.

Nor does Moran explicitly disclose compiling to form said binary programmable logic control program; however, Moran teach no source code for being loaded in memory for execution, only user program being loaded to support the BIOS system functionality of the controller (col. 6, line 59 to col. 7, line 3). Hence this compiling limitation is implicitly disclosed.

As per claim 6, see Moran (e.g. Fig. 2, 3, 9; *user storage ... emulation* - col. 5, lines 36-44; col. 5, line 46 to col. 6, line 48).

As per claim 7, Moran discloses a method comprising:

receiving from a communication/programming device a binary programmable logic control program (e.g. Fig. 2, 3, 9; *user storage ... emulation* - col. 5, lines 36-44; col. 5, line 46 to col. 6, line 48 - Note: flashed program stored at single chip controller implicitly discloses receiving a externally provided programmable code) at a single-chip execution device having a re-programmable memory (Fig. 3),

said communication/programming device separable from said single chip program execution device (Fig. 2 – Note: the user program being flashed into the controller 20 and fetched by controller OS reads on separate communication/programming device adapted to translate user program into application code, or executable form, externally provided and stored into controller programmable memory – see col. 6, line 59 to col. 7, line 3),

said binary control program comprising a compilation of a symbolic user program combined with a BIOS system support functions to form a single executable module, said single-chip execution device adapted to provide said single chip controller with operation system functions (see SUMMARY; col. 5, line 46 to col. 6, line 48) comprising sequencing the user program (e.g. col. 6, line 59 to col. 7, line 3 – Note: the loading of user program and BIOS functions to operate basic operation of device reads on a single module to effect basic I/O and power checking or OS diagnostics routines);

said single chip execution device adapted to execute said binary programmable logic control program to operate a programmable controller (e.g. SUMMARY; col. 5, line 46 to col. 6, line 48; col. 6, line 59 to col. 7, line 3),

said controller lacking a memory device separate from the single-chip execution device (e.g. Fig. 5 – controller with system memory 12 comprising flashed BIOS and separated and

executing independent from any external memory reads on lacking a memory device external to said execution device); and

loading said binary programmable logic control program into the re-programmable memory (Fig. 3) of said execution single chip device.

Moran does not explicitly disclose that the programmable single chip controller is a PLC. But this limitation has been addressed in claim 4 above.

Nor does Moran expressly disclose the BIOS support functions to operate the device OS are system support kernel combined with the compilation of the user program to form the binary programmable logic control program; this feature has been addressed in claim 4 above.

As per claim 8, this corresponds to claim 6 above, and is rejected likewise.

As per claim 9, Moran discloses a programmable controller system, comprising: within a single-chip, a program execution device having a re-programmable memory (e.g. Fig. 3), said device adapted to execute a binary programmable logic control program, said control program stored in said a re-programmable memory, said a binary programmable logic control program comprising a compilation of user program and BIOS system support (e.g. Fig. 2, 3, 9; *user storage ... emulation* - col. 5, lines 36-44; col. 5, line 46 to col. 6, line 48);

said binary programmable logic program adapted to operate a programmable controller (Fig. 2, 3, 9; *user storage ... emulation* - col. 5, lines 36-44; col. 5, line 46 to col. 6, line 48); said programmable controller program lacking a memory device separate from the single-chip execution device (e.g. Fig. 5);

a separable communication/programming device for providing functions required for external communication of said programmable control program, said binary control program

comprising a binary module formed from compiling a symbolic user program combined with a BIOS system support functions to form a single executable module (e.g. Fig. 2, 3, 9; *user storage ... emulation* - col. 5, lines 36-44, SUMMARY – Note: executable functions being flashed into execution device reads on compilation done externally and stored by said communication/programming device – See Fig. 2),

the BIOS functions adapted to provide said programmable controller with operation system functions (see SUMMARY; col. 5, line 46 to col. 6, line 48) comprising sequencing the user program (e.g. col. 6, line 59 to col. 7, line 3), said communication/programming device adapted to load said binary programmable logic control program into said re-programmable memory (Fig. 2-3); and wherein said binary control program is stored in said re-programmable memory of said execution device by direct manipulation of logic controls of said memory (e.g. col. 6, line 59 to col. 7, line 3; Fig. 7-8).

Moran does not explicitly disclose that the programmable single chip controller is a PLC. But this limitation has been addressed in claim 4 above.

Nor does Moran expressly disclose the BIOS support functions to operate the device OS are system support kernel combined with the compilation of the user program to form the binary programmable logic control program; this feature has been addressed in claim 4 above.

As per claim 10, only Stripf discloses a watchdog timer (e.g. Fig. 3-4) to complement to BIOS functions of Moran, this limitation would have been obvious by virtue of the rationale as to why kernel support function would enhance the I/O and power-up routines, OS diagnostics by Moran as set forth in claim 4.

As per claim 11, Moran discloses a computer-readable medium with stored therein instructions for executing:

receiving from a communication/programming device a binary programmable logic control program (e.g. Fig. 2, 3, 9; *user storage ... emulation* - col. 5, lines 36-44; col. 5, line 46 to col. 6, line 48 - Note: flashed program stored at single chip controller implicitly discloses receiving a externally provided programmable code) at a single-chip execution device having a re-programmable memory (Fig. 3), said single chip execution device adapted to execute a binary programmable logic control program stored in said re-programmable memory (e.g. Fig. 7,8);

said communication/programming device separable from said single chip program execution device (Fig. 2 – Note: the user program being flashed into the controller 20 and fetched by controller OS reads on separate communication/programming device adapted to translate user program into application code, or executable form, externally provided and stored into controller programmable memory – see col. 6, line 59 to col. 7, line 3),

said binary programmable logic control program adapted to operate a programmable controller (Fig. 2, 3, 9; *user storage ... emulation* - col. 5, lines 36-44; col. 5, line 46 to col. 6, line 48);

said binary programmable logic control program comprising a binary module formed from compiling a symbolic user program combined with a BIOS system support functions to form a single executable module (e.g. Fig. 2, 3, 9; *user storage ... emulation* - col. 5, lines 36-44, SUMMARY – Note: executable functions being flashed into execution device reads on compilation done externally and stored by said communication/programming device – See Fig. 2),

said BIOS system support functions adapted to provide said programmable controller with operation system functions (see SUMMARY; col. 5, line 46 to col. 6, line 48) comprising sequencing the user program (e.g. col. 6, line 59 to col. 7, line 3 – Note: the loading of user program and BIOS functions to operate basic operation of device reads on a single module to effect basic I/O and power checking or OS diagnostics routines);

said programmable controller lacking a memory device separate from the single-chip execution device (e.g. Fig. 5 – controller with system memory 12 comprising flashed BIOS and separated and executing independent from any external memory reads on lacking a memory device external to said execution device).

Moran does not explicitly disclose compiling at the communication/programming device for form the OS/BIOS support programmable logic control program. But in view of the flash memory for storing executable and the host computer from Fig. 2-3; this externally compiled code is disclosed.

Moran does not explicitly disclose that the programmable single chip controller is a PLC. But this limitation has been addressed in claim 4 above.

Nor does Moran expressly disclose the BIOS support functions to operate the device OS are system support kernel combined with the compilation of the user program to form the binary programmable logic control program; this feature has been addressed in claim 4 above.

Response to Arguments

4. Applicant's arguments filed 5/2/2005 have been fully considered but they are persuasive. Following are the Examiner's observations in regard thereto.

(A) Applicant has submitted that the use of Agrawal has been treated as it were from Moran. It is to Office duty to be thankful to Applicant for the above understanding because there was indeed a typo error from the Office Action, which should have been Moran.

(B) Applicant has submitted that Moran uses 3 chips (Appl. Rmrks, pg. 7, bottom) without further evidence supporting this allegation with respect to the cited portions of Moran. It is noted that the rejection has cited a single integrated chip (ASIC). Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

(C) The **declaration under 37 CFR 1.132 filed 5/2/2005** is insufficient to overcome the rejection of claims 4-11 based upon a rejection using Moran under 35 USC §103 as set forth in the last Office action because it refer(s) only to the system described in the above referenced application and not to the individual claims of the application. Thus, there is no showing that the objective evidence of nonobviousness is commensurate in scope with the claims. See MPEP § 716. Following are the observations in regard thereto.

Applicant has submitted that expert knowledge provided by Affidavit 1.132 has it be established that Moran's integrated controller would not be found by one skill in the art to have taught 'programmable logic controller' or PLC (Appl. Rmrks, pg. 7, bottom). Let's assume for a moment that the Affidavit as submitted is conforming to the rules for USC 1.132 and contains expert knowledge showing insight on the question of obviousness or inherent teachings. The affidavit mentions about a definition as of 10/26/2000 and put forth that a PLC as being a 'device used to automate monitoring and control of industrial plant'. This argument amounts to

clarifying on a field of application limitation that is not claimed. Besides, Moran is not explicitly teaching a actual PLC; but provides a integrated controller in a single chip (see Fig. 3,6), thus has shown sufficient teaching that such chip is a controller. The intended use of such integrated controller can include manipulating of data with complex operations or control of industrial switching of devices, but that is not the intended use that made Moran's become a patent, nor does it impart any patentable weight even if claimed in this instant application. The rejection has made it clear that providing functionalities of a controller inside a integrated chip is suggestive of usage of such chip to make it a actual PLC, which becomes the ground to bring Stripf's PLC usage and the rationale as to combine in a USC §103(a) section. This is not an anticipation type of rejection per se; and in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The arguments provided by the Affidavit do not amount to put forth the deficiencies of a obviousness type of combination but appear to contend with 'one skill in the art' would not have found Moran's circuit package to expressly or inherently teach, which is otherwise more geared to address anticipation and hence out of context.

(D) Applicant has submitted from the Office Action, that Moran's kernel support is considered as implied or inherent; that Moran's separable communication device is being disclosed by apparent inherency; that Moran's loading of code implies that compiling has been disclosed (Appl. Rmrks, pg. 9, top 3 para). First, the rejection has pointed to parts that shows that the flash program comprise operating system that will be loaded upon BIOS and power up

routines. And this illustrates why a kernel is being perceived as being part of the program being stored in the flash. It is a well-known concept that any operating system in order to start functioning requires a basic set of core code integral to it; and that is a kernel. Some books even analogize an OS to a kernel itself, because one cannot exist without the other. And the rejection has also provided the grounds as to why a kernel support functionality being included in the flash code to operate a PLC as by the teaching from Stripf would have rendered this operating system kernel an obvious feature to enable normal operation of a controller as endeavored by Moran. Second, the teaching by Moran concerning a program code being flashed has been questioned for not providing sufficient ground for inherency. From the language of the claim the recited 'separable communication/programming device' encompasses a separable communication device or a separable programming device, both adapted to convert code. Based on Moran's single package chip controller, there is no other reasonable way to perceive that this chip can include either a compiling functionality or a integral utility able to convert code into becoming a firmware module. The very fact that the OS support program has been flashed into the chip dictates that the chip is the recipient of code that has been prepared external to the confines of the chip; and one skill in the art when faced with a single chip being flashed with an executable as in Moran's method would easily recognize that some external system has been adapted with utilities for generating a program in order to communicate the ready made executable into the flash memory, e.g., by means of network or bus transfer or manufacturer burn-in. For example, a manufacturer equipped with compiling subsystem to provide the firmware, and using burn-in method to embody the firmware code into the chip, would have read on a compiling device external to the programmable controller chip. Hence, there is sufficient ground to acknowledge

that the teaching as required from the claim has been met; and Applicant has failed to point out specifics in the Moran reference showing that Moran's flash program necessarily entails a compiling utility internal to such package controller.

(E) Applicant has submitted that Moran does not teach a programmable logic controller I/O functions (Appl. Rmrks, pg. 9, bottom para). The USC 103 rejection does not address a I/O functions features but mainly focuses on rendering the making of a controller into a PLC an obvious limitations. There is no remote allusion to an expressed or inherent teaching by Moran concerning a PLC from the rationale as set forth in the rejection because this rejection is a combination of teachings according to prima facie, and not one single reference is to be attacked individually. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

(F) Applicant has submitted that a single chip program execution in Stripf would render Stripf inoperative by virtue of the declaration para. 33-38 by Dr Williams (Appl. Rmrks, pg. 10, top 4 para).

The **declaration under 37 CFR 1.132 filed 5/2/2005** is insufficient to overcome the rejection of claims 4-11 based upon a rejection using Moran under 35 USC §103 as set forth in the last Office action. Following are the reasons why.

First, the date 10/26/2000 used by the argument as priority date of the Application is erroneous because the effective date therefor should be 10/26/1999. Second, as established in para 34 of the affidavit, the PLC definition for establishing a 'industrial plant' limitation has been addressed in section C above. Third, from paras 35-38 argument that Stripf's PLC execution software blocks would require continually reloading or dynamically tied up. The

rationale of the USC §103 is to provide reasons as to make Moran's integrated chip with burn-in flash program to operate like a PLC as used in manufacturing activities as mentioned by Stripf. It is noted that Moran's integrated chip can be used for loading code from many retrofitting means, which signifies that it is not expressly confined to just one-time type of burn-in (see col. 2 of Moran). The manufacturing facilities as shown in Stripf's col. 2 may as well be adapted to provide code linkage to an integrated chip of Moran if the latter chip is purported by the manufacture to perform a PLC type of function. More importantly, the affidavit remarks do not appear to build their ground based on the claimed language. There is no convincing evidence from the claim or from Moran that would render the integrated chip unfit to be used as a PLC; and there no teaching anywhere in the claim that enforces a PLC code being necessarily dynamically relinked as opposed to a code flashed into a chip; and there is no teaching anywhere in Moran or in Stripf that dictates that once a program is flashed, a flash program cannot be utilized in a PLC (**) . The claim even recites 'firmware' which is exactly what a Flash memory is purported to embody. The very fact of having manufacturing sites to support change in the controller program by Stripf would be considered equal in purpose to the retrofitting endeavors by Moran (see Moran: SUMMARY) when simple program accommodation per operating system can be provided via likely manufacturer-based flash memory data erasing/writing techniques. The references have to be viewed in light of this common endeavor or equal purpose. It has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case,

there is a common endeavor in combining the teachings by Stripf and Moran; that is to accommodate a program for different requirement once the product is distributed. Moreover, the argument from the Affidavit does not appear to take into consideration the extent to which the teachings as claimed have been conveyed/interpreted to one skill in the art (refer to ** from above) because it refer(s) only to the system described in the above referenced application and not to the individual claims of the application. Thus, there is no showing that the objective evidence of nonobviousness is commensurate in scope with the claims. See MPEP § 716.

For the above reasons, the claims will stand rejected as set forth in the Office Action.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)272-3719.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence – please consult Examiner before using) or 703-872-9306 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT
June 15, 2005

ANIL KHATRI
PRIMARY EXAMINER